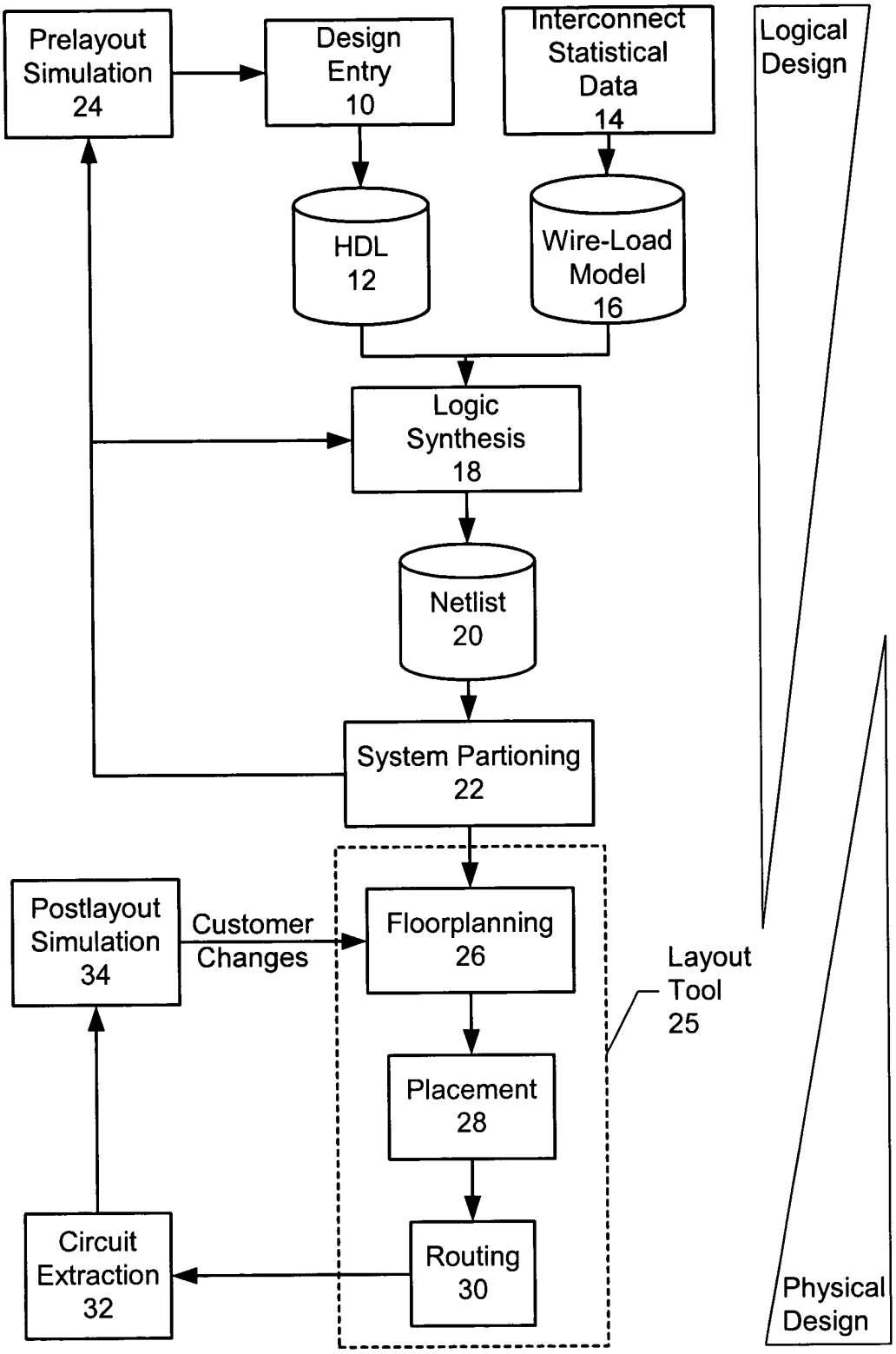

ASIC Design Flow

FIG. 1

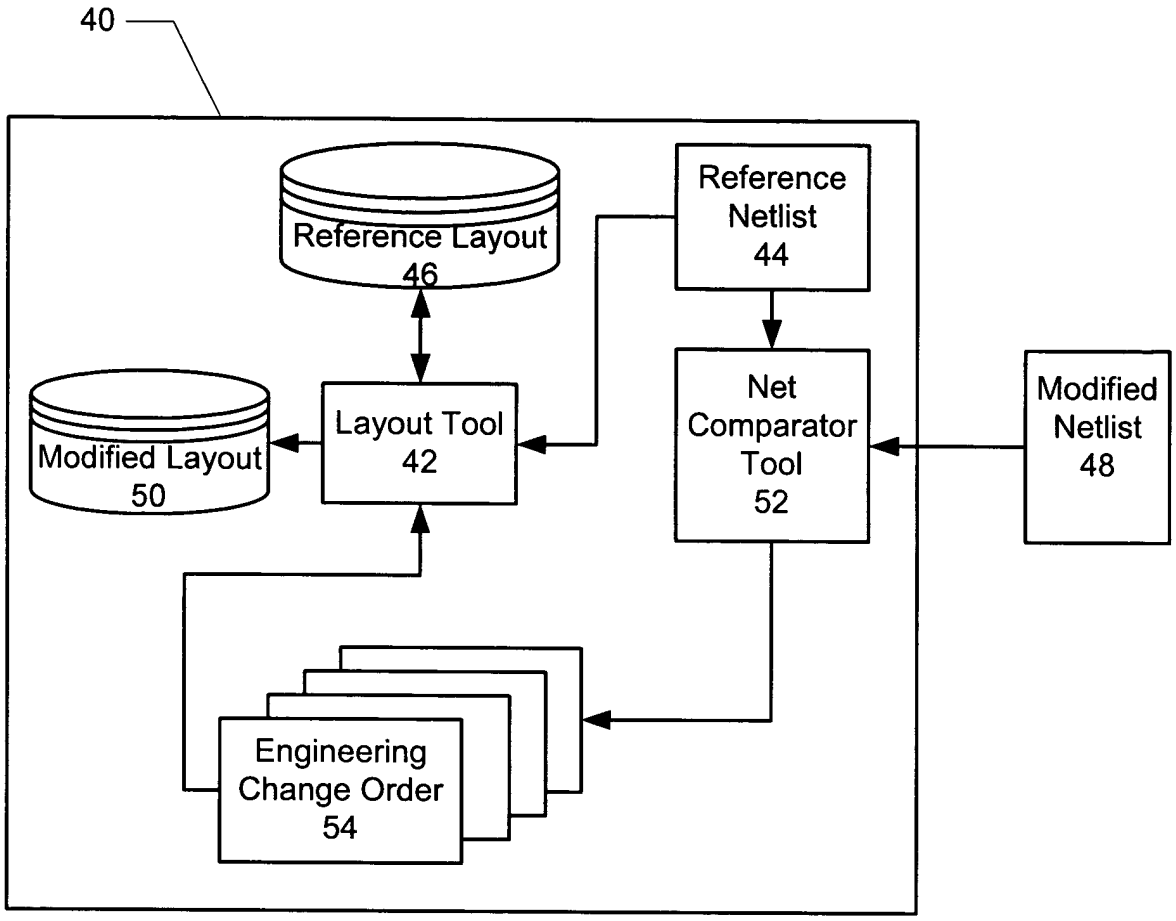
40
Reference Layout
46
Reference
Netlist
44
Modified Layout
50
Layout Tool
42
Net
Comparator
Tool
52
Modified
Netlist
48
Engineering
Change Order
54

FIG. 2

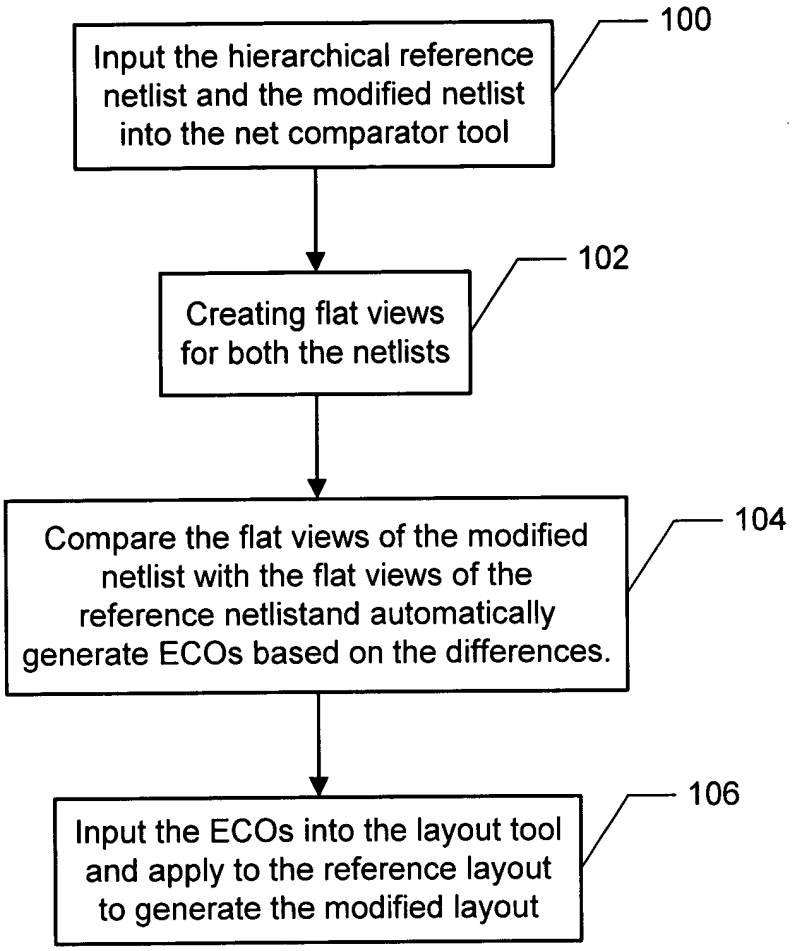
Input the hierarchical reference netlist and the modified netlist into the net comparator tool
100
Creating flat views for both the netlists
102
Compare the flat views of the modified netlist with the flat views of the reference netlistand automatically generate ECOs based on the differences.
104
Input the ECOs into the layout tool and apply to the reference layout to generate the modified layout
106

FIG. 3

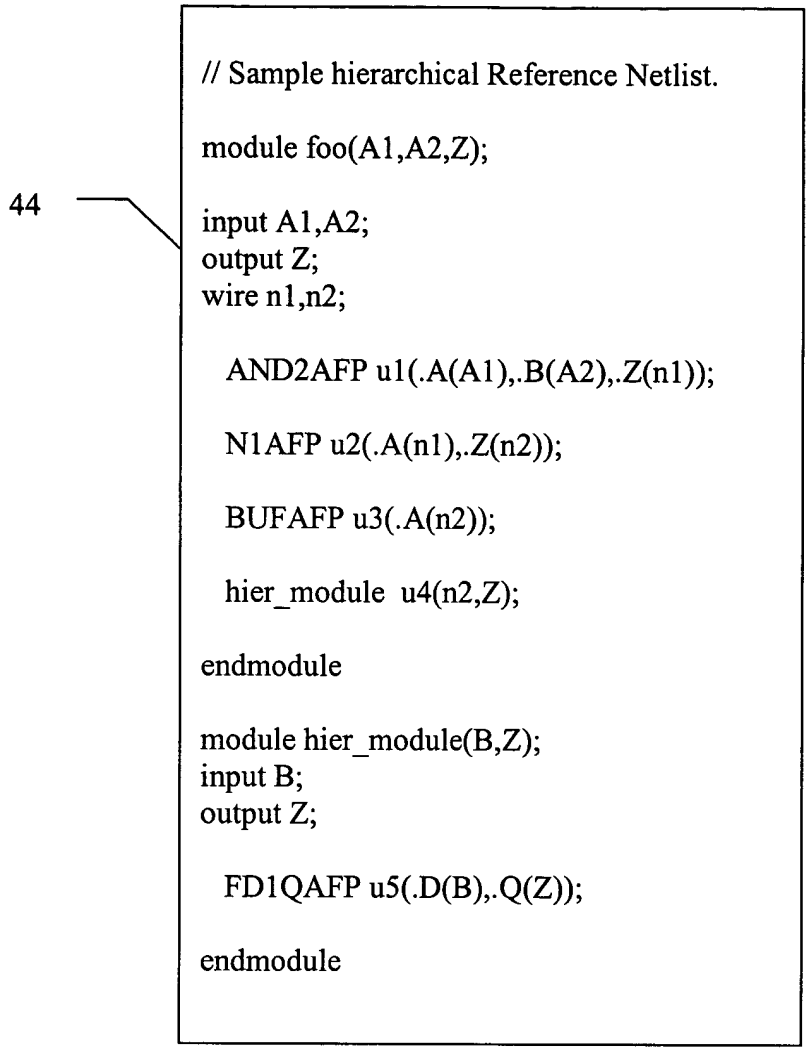
44
// Sample hierarchical Reference Netlist.
module foo(A1,A2,Z);
input A1,A2;
output Z;
wire n1,n2;
AND2AFP u1(.A(A1),.B(A2),.Z(n1));
N1AFP u2(.A(n1),.Z(n2));
BUFAFP u3(.A(n2));
hier_module u4(n2,Z);
endmodule
module hier_module(B,Z);
input B;
output Z;
FD1QAFP u5(.D(B),.Q(Z));
endmodule

FIG. 4A

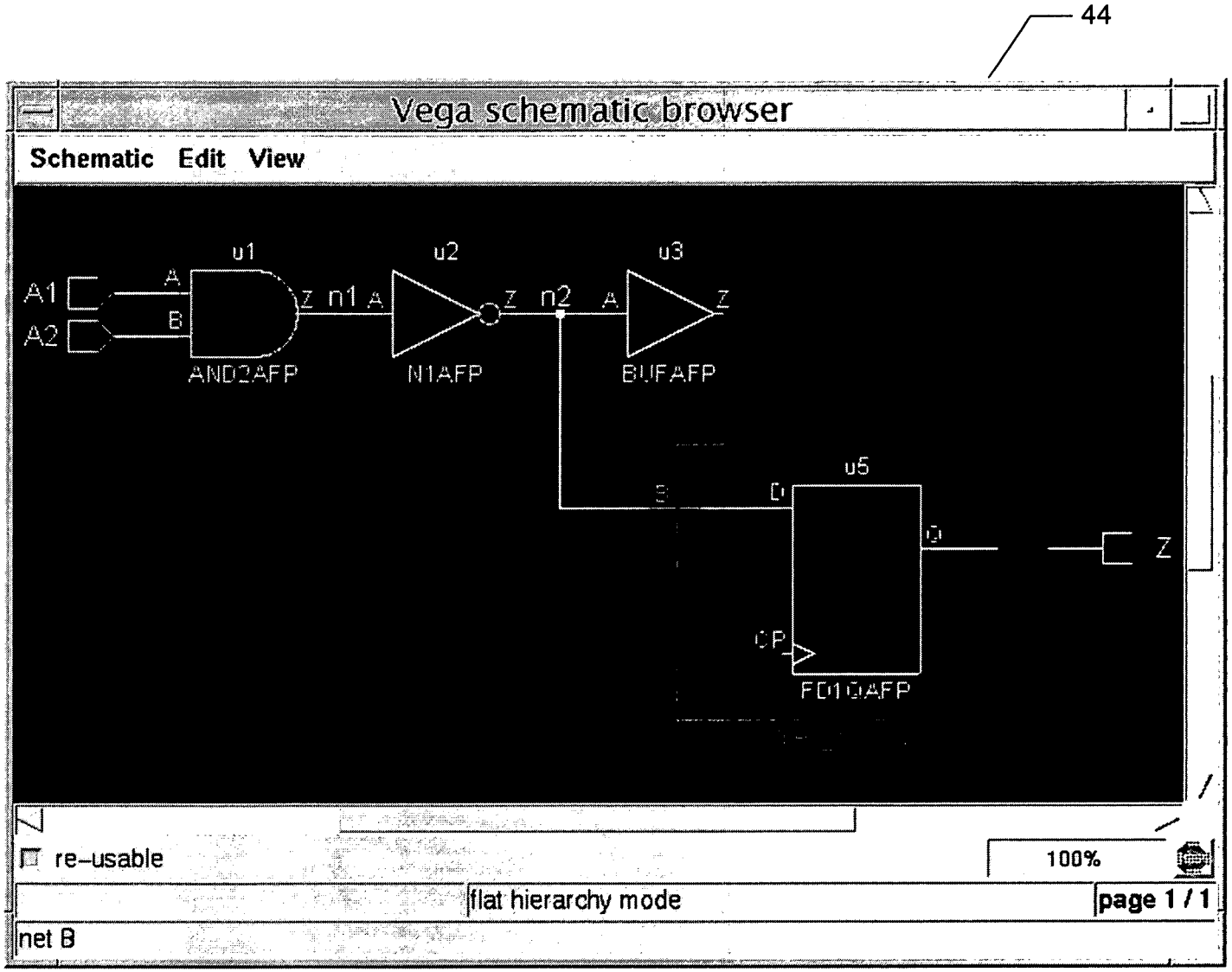
44
Vega schematic browser
Schematic Edit View
u1
u2
u3
A1
A2
A
B
Z
n1
n2
AND2AFP
N1AFP
BUFAFP
u5
D
Q
CP
FD1QAFP
re-usable
100%
flat hierarchy mode
page 1 / 1
net B

FIG. 4B

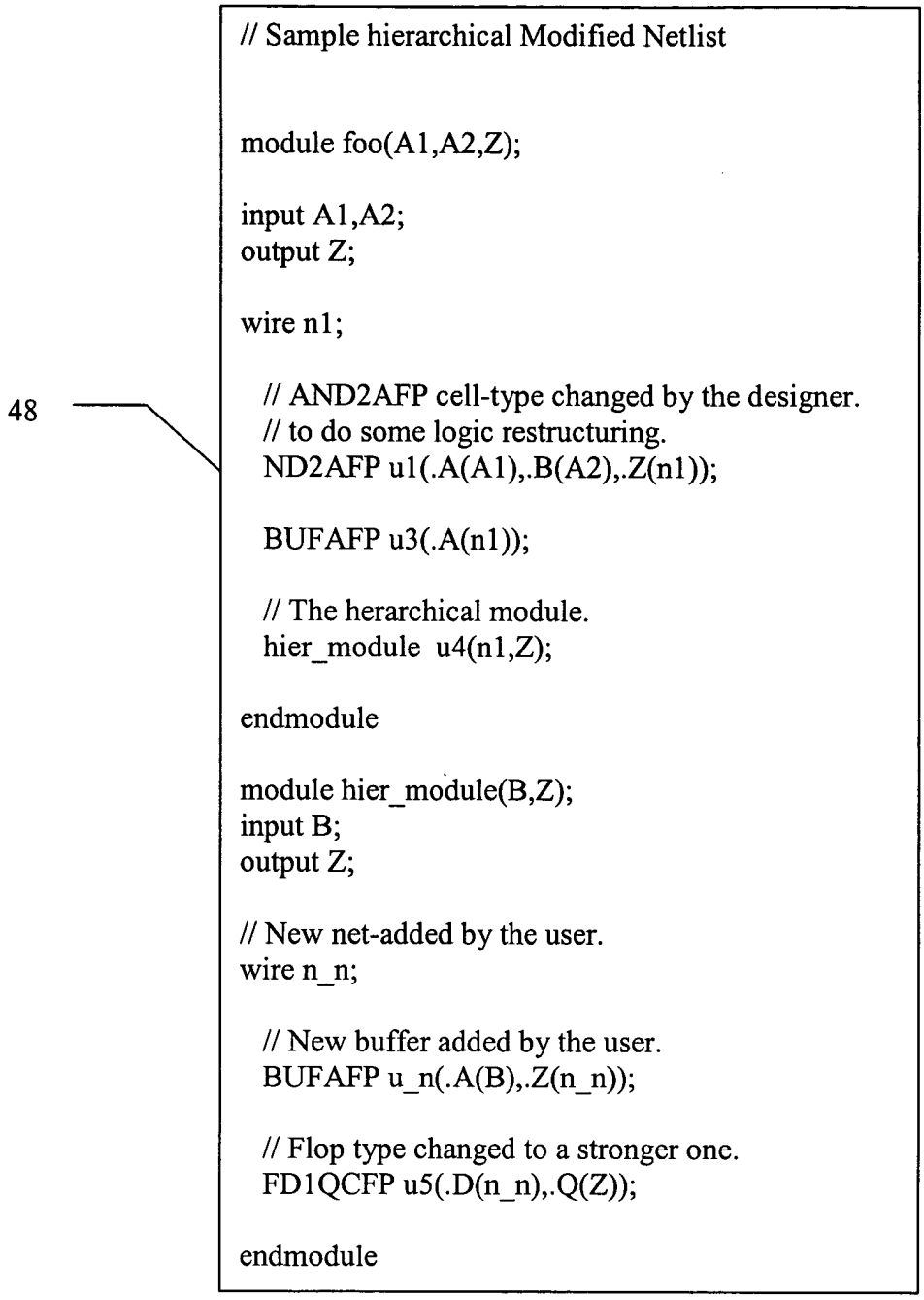
// Sample hierarchical Modified Netlist
module foo(A1,A2,Z);
input A1,A2;
output Z;
wire n1;
// AND2AFP cell-type changed by the designer.
// to do some logic restructuring.
ND2AFP u1(.A(A1),.B(A2),.Z(n1));
BUFAFP u3(.A(n1));
// The herarchical module.
hier_module u4(n1,Z);
endmodule
module hier_module(B,Z);
input B;
output Z;
// New net-added by the user.
wire n_n;
// New buffer added by the user.
BUFAFP u_n(.A(B),.Z(n_n));
// Flop type changed to a stronger one.
FD1QCFP u5(.D(n_n),.Q(Z));
endmodule
48

FIG. 5A

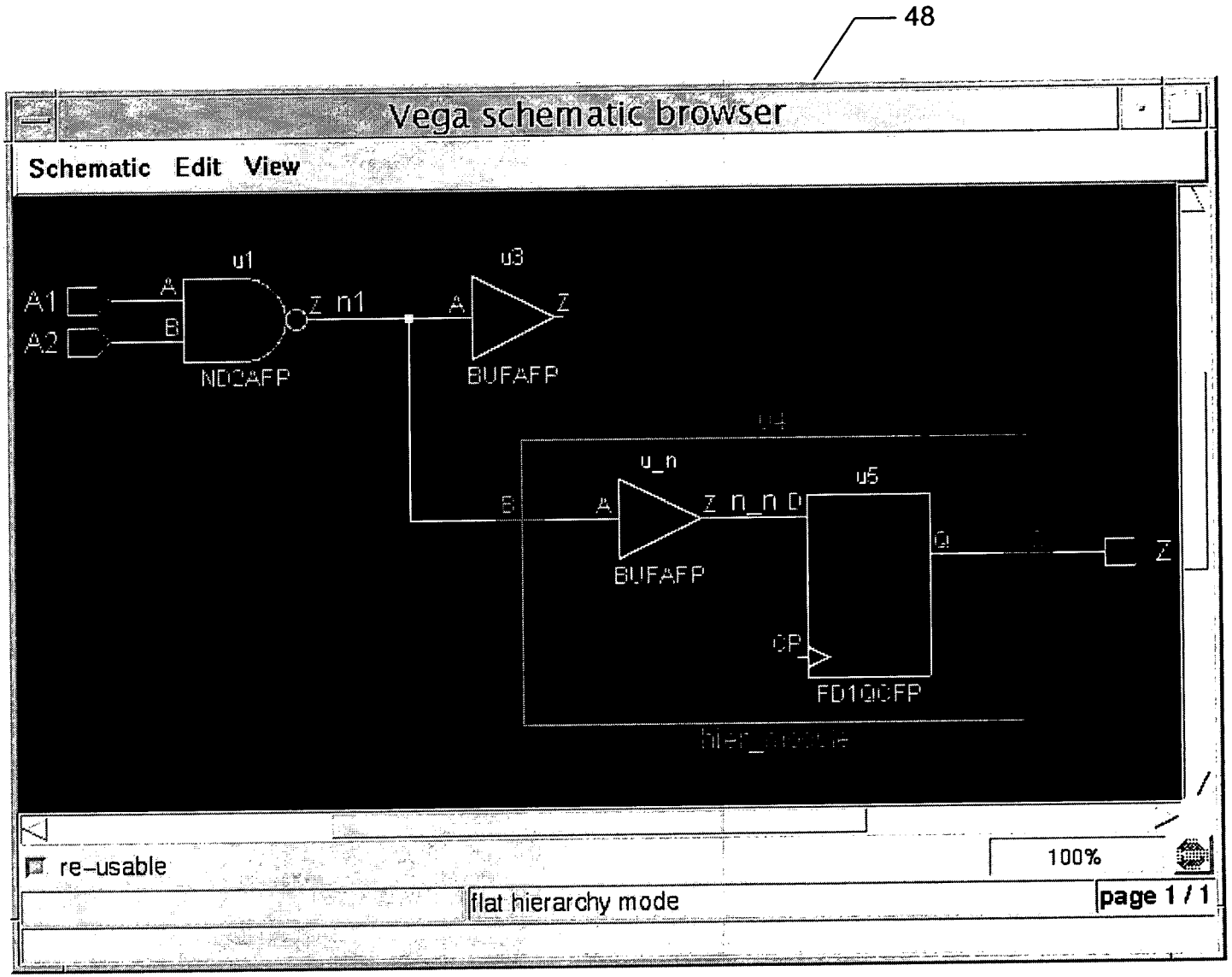
48
Vega schematic browser
Schematic Edit View
u1
A1
A2
A
B
Z n1
ND2AFP
u3
A
Z
BUFAFP
u4
u_n
B
A
Z n_n 0
BUFAFP
u5
Q
Z
CP
FD1QCFP
re-usable
100%
flat hierarchy mode
page 1 / 1

FIG. 5B